

REMARKS

Claims 19-20 are pending in the application. Claim 19 is independent. In the present paper, no claims have been amended, canceled, or added. These changes are believed to introduce no new matter and their entry is respectfully requested.

Rejection of Claims 19-20 Under Obviousness-Type Double Patenting

In the Office Action, the Examiner rejected claims 19-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,778,548 to Burton, et al. (hereinafter "*Burton I*"). Applicants respectfully traverse the rejection. In papers filed herewith, Applicants have submitted a Terminal Disclaimer disclaiming the terminal part of any patent granted on the above-identified patent application that would extend beyond the expiration of the full statutory term of U.S. Patent No. 6,778,548. Applicants respectfully submit that the Terminal Disclaimer overcomes the obviousness-type double patenting rejection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 19-20.

Provisional Rejection of Claims 19-20 Under Obviousness-Type Double Patenting

In the Office Action, the Examiner rejected claims 19-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent Publication No. 2004/0151176 to Burton, et al. (hereinafter "*Burton II*"). Applicants respectfully traverse the rejection. In papers filed herewith, Applicants have submitted a Terminal Disclaimer disclaiming the terminal part of any patent granted on the above-identified patent application that would extend beyond the expiration of the full statutory term of U.S. Patent Publication No. 2004/0151176. Applicants respectfully submit that the Terminal Disclaimer overcomes the obviousness-type double patenting rejection. Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 19-20.

Rejection of Claims 19-23 Under 35 U.S.C. §103(a)

In the Office Action, the Examiner rejected claims 19-20 under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 5,598,541 to Malladi et al. (hereinafter "*Malladi*") in view of

U.S. Patent No. 6,801,535 to Richards et al. (hereinafter “*Richards*”). Applicants respectfully traverse the rejection.

To establish a *prima facie* case of obviousness, an Examiner must show that there is some expectation of success that the combination proffered would result in the claimed invention. The Examiner also must show that the cited references teach each and every element of the claimed invention. (MPEP §2143.) *citing In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). A patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was independently known in the prior art. *KSR Int’l C. v. Teleflex, Inc.*, No 04-1350 (U.S. Apr. 30, 2007). It can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the prior art elements in the manner claimed. (*Id.*)

Independent claim 19 recites in pertinent part “first circuitry to generate a packet header ***based on payload data*** received from a micro-engine or from a memory controller, the first circuitry comprising: second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in first-in first-out (FIFO) circuitry” (emphasis added). In the Office Action, the Examiner states that *Malladi* discloses in Figures 3 and 5 and at column 7, line 30, to column 8, line 15, “first circuitry to generate a packet header based on payload data received from a micro-engine or from a memory controller, the first circuitry comprising: second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in first-in first-out (FIFO) circuitry” as recited in claim 19. Applicants respectfully disagree.

Applicants respectfully submit further that the Examiner has failed to make out a *prima facie* case of obviousness of claim 19 with respect to *Malladi* because the Examiner has failed to demonstrate how *Malladi* teaches the each and every element recited in claim 19. For example, the Examiner has not shown where *Malladi* discloses “first circuitry to generate a packet header ***based on payload data*** received from a micro-engine or from a memory controller, the first circuitry comprising: second circuitry to receive packet data from the memory controller or the micro-engine, and to store the packet data in first-in first-out (FIFO) circuitry” as recited in

claim 19. The Examiner points to no teaching in *Malladi* that discloses *how* a packet is generated. Applicants respectfully submit that the cited portions of *Malladi* provide no such disclosure. Nor does any other portion of *Malladi* disclose how a packet is generated. Accordingly, Applicants respectfully submit therefore that claim 19 is patentable over *Malladi*.

Claim 20 properly depends from claim 19 and is thus patentable for at least the same reasons that claim 19 is patentable. (MPEP § 2143.03 (citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)). Accordingly, Applicants respectfully request that the Examiner reconsider and remove the rejection to claims 19-20.

CONCLUSION

Applicants respectfully submit that all grounds for rejection have been properly traversed, accommodated, or rendered moot and that the application is now in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

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I hereby certify that this correspondence is being submitted electronically via EFS-Web on the date shown below.

9/19/2007
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